

Applicant(s) : Hideki Hirayama
Serial No. : 10/783,500
Filed : February 20, 2004
Page : 6 of 8

Attorney Docket No.: 35901-078001
Client Ref. No.: P1S2003323US

Remarks

We acknowledge the Examiner's indication that claims 7, 8, and 10 are allowed. We have also amended claims 9 and 10 to recite "the second clock signal" to provide proper antecedent basis.

§103 Rejections

The Examiner rejected claims 1-3, 5, 6, and 9 as being unpatentable over Tobita et al. (US patent 6,385,257 B1) in view of Hase et al. (US patent 5,937,020). Tobita fails to disclose a digital PLL circuit and a demodulator connected to a digital PLL circuit and an analog PLL circuit. The Examiner also acknowledges that Tobita does not disclose a demodulator that is configured to be able to switch between first and second control signals. The Examiner argues that these missing features are disclosed by Hase. Specifically, the Examiner argues that Hase discloses a digital PLL circuit 3 and points to the combination of Hase's synchronizing clock generator 2 and timing controller 43 as meeting the limitations of a demodulator that is configured to be able to switch between first and second control signals, as required by claim 1. The Examiner states that it would have been obvious "to incorporate both the analog and digital PLL's of Hase into the decoder of Tobita" (page 3).

We have reviewed the Tobita and Hase patents and do not believe that either Tobita or Hase, separately or in any proper combination, describe or suggest a system comprising ... a demodulator, connected to a digital PLL circuit and a analog PLL circuit and configured to be able to switch between first and second clock signals, the demodulator sampling the wobble signal using either the first clock signal or the second clock signal to demodulate the address information on the optical disk, as recited in amended claim 1.

Tobita teaches a decoder based on an analog PLL and Hase discloses a digital PLL circuit as well as a demodulator that is connected to both digital and analog PLL circuits. Although Tobita use a wobble signal, there is no need for switching because, as appreciated by the Examiner, there is only an analog PLL circuit. Although Hase

discloses both an analog and a digital PLL, switching is not performed by clock signals.

Rather, Hase states:

“there is arranged a timing control circuit 43 for creating a change-over timing signal (indication signal) to invoke either one of the operations of the analog and digital PLL circuits” (column 9 lines 22-25).

The timing control circuit is activated by the hard disc controller; it does not sample the input signal. Even assuming that it would have been obvious to apply Tobita's use of a wobble signal to Hase's circuit containing both an analog PLL and a digital PLL, one still would not have arrived at the idea of using the wobble signal to control the generation of a change-over timing signal.

We therefore submit that claim 1 is allowable, as it is not an obvious combination of the prior art.

Since claims 2, 3, 5, 6, and 9 depend from claim 1, we submit that they are also patentable for at least the same reason that claim 1 is allowable.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

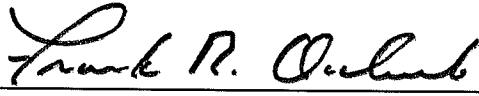
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Page : 8 of 8

Attorney Docket No.: 35901-078001
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No fees are believed to be due, however, please apply any other charges or credits to Deposit Account No. 50-4189, referencing Attorney Docket No. 35901-078001.

Respectfully submitted,

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